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Capacitor Multiplier with One Transconductor Cell

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***Abstract*—A new programmable capacitance multiplier implementation is presented in this paper. It is based on a fairly known architecture, but the proposed circuit employs only one linear transconductor (Gm cell). The mathematical analysis of the new capacitance multiplier is presented along with simulations performed on a circuit implemented in standard 0.18-µm CMOS process. Two applications are also presented: a triangular waveform generator and a fully differential lossy integrator, both with emulated capacitances programmable over three octaves.**

***Keywords*— capacitor multiplier, current mode, transconductor, analog integrated circuits**

1. Introduction

In general, the integration of capacitances larger than hundreds of picofarads is not feasible/desired in general-purpose integrated technologies, due to the large die area they require. Using external capacitors is not always acceptable, as this implies dedicated pins and obviously increases the bill-of-materials (BoM) for the application.

Another option is the implementation of a circuit that emulates the features of a large capacitance while actually employing a placed/integrated capacitor many times smaller than the emulated value – that is, a capacitance multiplier. In this case, it is often required to provide means for adjusting or programming the capacitance gain factor (G), at least in order to compensate for variations of the process, supply voltage and temperature (PVT).

Several circuit solutions for implementing capacitance multipliers have been reported in the open literature. Most of them are based on the Miller effect; thus, they can be classified as a voltage mode approaches. Their performance is usually hindered by signal swing limitations since the maximum voltage applied to the capacitance is reduced by the gain factor, G. Current mode approaches are faster and have a wider dynamic range [1].

The principle of current mode approach is shown in Fig. 1. It is based on a simple current mirror, which senses the current passing through the placed capacitor (C) and scales it by the current gain, K. This way, the equivalent capacitance is seen at the output of the current mirror appears G=(K + 1) larger than C. However, most circuits reported in literature provide a very low-quality factor, Q, for the resulting multiplied capacitance, mainly due to the relatively large input resistance of the current mirror, Rin = 1/gm [2]. Other current mode implementations use second-generation current conveyors as active devices to multiply the capacitance but they do not allow a variable capacitance multiplication factor [3].

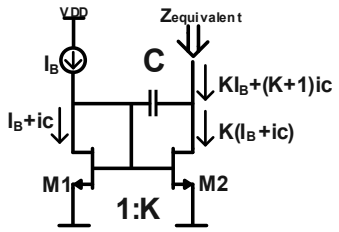

Fig. 1 Current mode approach for capacitor multiplier.

A typical solution for a capacitor multiplier is the circuit presented in [4]. The circuit presented in Fig. 2 a), uses two transconductance amplifiers (OTAs) with transconductance gains gm_1 and gm_2. The transconductance of OTA_2 ca be adjusted by means of a control voltage or a bias current. One terminal of capacitor C is connected to OTA_1. OTA_1 uses unity gain negative feedback and operates as a low-value series resistor $R_1=1/Gm_1$ connected between the remaining capacitor terminal and ground.

The equivalent circuit with its series resistor R_1 is presented in Fig. 2 b). For a purely capacitive behavior ($Q=\infty$) the value of R_1 should be zero. In order to achieve a high Q, OTA_1 should have a large gm while OTA_2 should have a large output resistance.

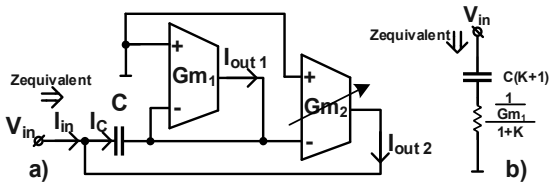

Fig. 2 a) Capacitor multiplier with two transconductor cells; b) equivalent circuit [4].

2. Proposed circuit

The proposed capacitance multiplier scheme presented in Fig. 3 contains only one transconductance core (common Gm core) and multiple scaled output stages that emulates the two OTAs [5]. The Gm core is based on Kwan-Martin transconductor topology [6], presented in Fig. 4 and optimized for high linearity and accuracy whose transconductance is determined by:

$$\mathrm{Gm} = \frac{2A_{ii}}{R_{deg}} \qquad (1)$$

where $A_{ii}=(W/L)_{M3}/(W/L)_{M2}$.

The inputs of the two OTAs are connected in parallel, for this reason, we can write:

$$\mathrm{Vin_{Gm1}} = \mathrm{Vin_{Gm2}} = -\frac{I_C}{Gm_1} \qquad (2)$$

$$I_{out2} = Gm_2 \mathrm{Vin_{Gm2}} = -\frac{Gm_2}{Gm_1} I_C \qquad (3)$$

$$I_{in} = I_C - I_{out2} \qquad (4)$$

If we note the ratio of the two transconductors with $K=Gm_2/Gm_1$, the equivalent input impedance is:

$$Z_{equivalent} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{I_C(1+K)} \qquad (5)$$

and the equivalent capacitance is:

$$C_{equivalent} = C(1+K) = C * G \qquad (6)$$

The proposed circuit was implemented in a standard 180nm technology. The stand-alone capacitor multiplier circuit was simulated for a 5pF base capacitor and a 1mS Gm core.

The variable output stage was set in order to obtain a Gm_2/Gm_1 ratio of K=1, 3, 7 and 15 for a $C_{equivalent}=C(1+K)$ =10pF, 20pF, 40pF and 80pF. Fig. 5 a) presents the simulation

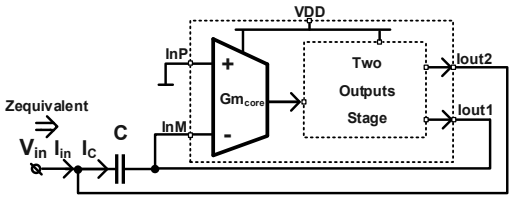

Fig. 3 Block diagram of the proposed capacitor multiplier with common-core and multiple outputs.

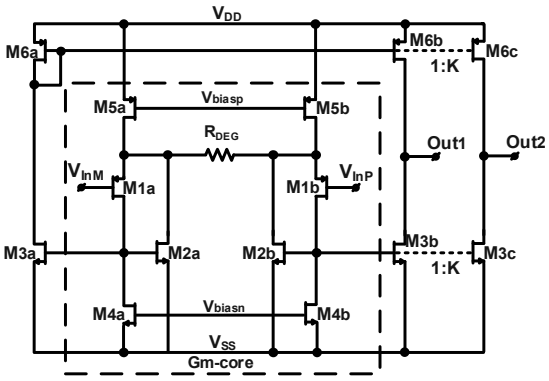

Fig. 4 Linear Gm-cell with two outputs based on the Kwan-Martin Gm-core [6] (shown within the dotted rectangle).

results of the AC response of the input and capacitor impedance for the circuit in which the output stage was implemented with active cascode, similar to [7]. Table I comprises a comparison between the performances of the proposed circuit and other works.

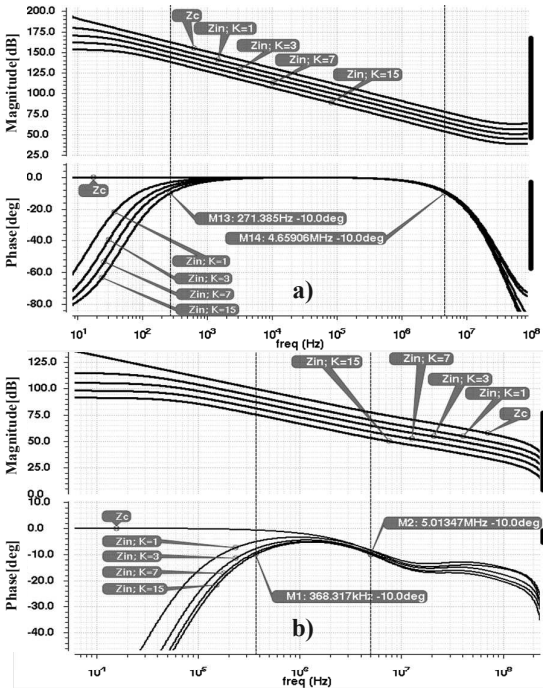

Fig. 5 AC response of the equivalent input impedance (magnitude and phase) for K=1, K=3, K=7, K=15 and capacitor impedance, a) with active cascode [7], b) with standard, one-level cascode.

TABLE I. PERFORMANCES COMPARISON : PROPOSED CAPACITOR MULTIPLIER VERSUS REFERENCES

	[4]	[8]	This work
Placed capacitor	800pF	0.1pF	5pF
Frequency range	3 decades* 1KHz-1MHz	2 decades* 10KHz-1MHz	3 decades** 1.9KHz-4.65MHz
Control	Variable current	Variable voltage	Programmable current
Process	discrete	180nm	180nm

* Based only on magnitude response, phase error not known; ** Phase error <10º

The active cascode is a closed loop structure that employs a gain stage to drive the gate of the cascode. It increases significantly the equivalent output impedance. For comparison, Fig. 5 b) presents the simulation results for the circuit with standard cascode implementation.

3. Applications for capacitor multiplier

A. Triangle-wave generator with adjustable frequency

For large-signal application of the capacitor multiplier, a triangle waveform generator (oscillator) was implemented using the proposed schematic from above. The block diagram of the oscillator is shown in Fig. 6.

The oscillating frequency is given by:

$$f_{OSC} = \frac{I_B}{2C_{equivalent}\Delta V_{th}} \quad (7)$$

$$\Delta V_{th} = V_{thH} - V_{thL} \quad (8)$$

The oscillator was designed for a 7.5pF placed capacitor, and 200mVpp amplitude. The charge/discharge current was set top 15µA, according to equation (7).

Table II summarizes the results for the oscillating frequency of the proposed triangle waveform generator.

Fig. 7 illustrates the triangle-wave voltage across the capacitor for K=1 and K=15 which corresponds to the min and max frequency.

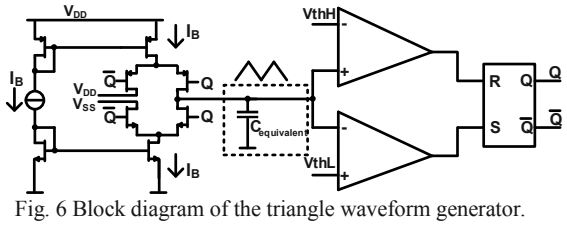

Fig. 6 Block diagram of the triangle waveform generator.

TABLE II. OSCILLATING FREQUENCY FOR SEVERAL VALUES OF THE K=GM_2/GM_1 RATIO - SIMULATION RESULTS

K ratio	Parameter		
	$C_{equivalent}$	f_{osc} *simulated*	f_{osc} *error*
1	15 pF	2.2 MHz	12%
3	30 pF	1.16 MHz	7%
7	60 pF	600 KHz	4%
15	120 pF	305 KHz	2.5%

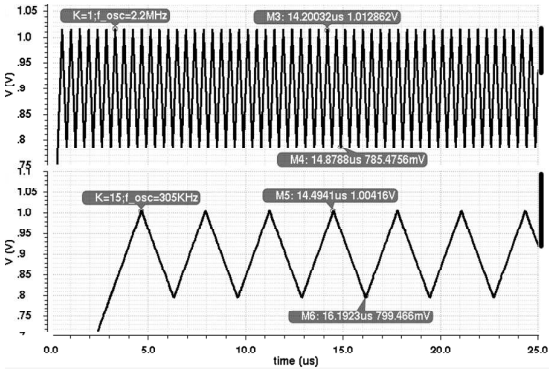

Fig. 7 Oscillator output, Vcap, for K=1 and K=15.

B. Fully differential lossy integrator with programmable pole frequency

For small-signal application of the capacitor multiplier, a fully differential, adjustable bandwidth, lossy integrator (Gm-C) was implemented using the proposed schematic with common-core and multiple output stages. The integrator block diagram is illustrated in Fig. 8 a).

For calculating the integrator bandwidth (-3dB cut-off frequency) the equivalent circuit depicted in Fig. 8 b) was used, where:

$$R_3 = \frac{1}{Gm_3};\ R_S = \frac{1}{Gm_1 + Gm_2} \quad (9)$$

The transfer function of the circuit is:

$$\frac{V_{out}}{V_{in}} = \frac{1 + sC\left(1 + \frac{Gm_2}{Gm_1}\right)\left(\frac{1}{Gm_2 + Gm_1}\right)}{1 + sC\left(\frac{1}{Gm_3} + \frac{1}{Gm_2 + Gm_1}\right)} \quad (10)$$

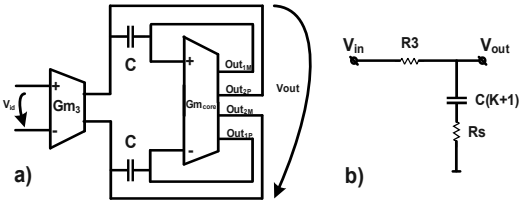

Fig. 8 a) Fully differential Gm-C integrator with capacitor multiplier; b) Equivalent circuit of the integrator.

Fig. 9 presents the AC magnitude characteristics of the integrator for four values of the current gain K, while in Fig. 10 the transient response of the integrator for a 40mVpp sine voltage 50KHz and 200KHz is presented. Table III summarizes the results for the -3dB cut-off frequency of the proposed integrator.

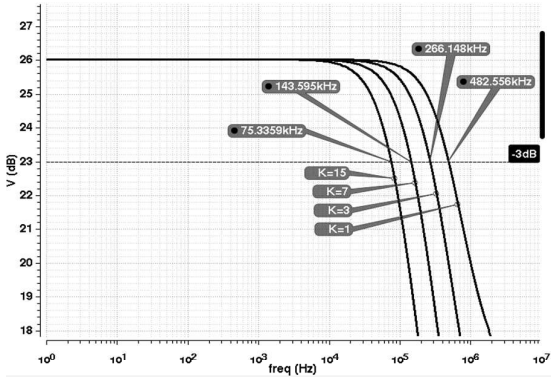

Fig. 9 AC response (magnitude) of the Gm-C integrator for K=1, K=3, K=7 and K=15.

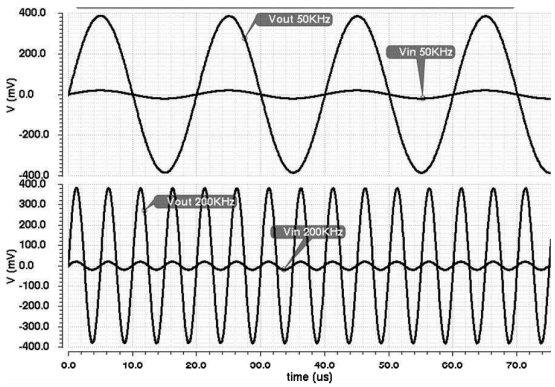

Fig. 10 Integrator transient output voltage for 50KHz input sine-voltage and output voltage for 200KHz input sine-voltage.

TABLE III. INTEGRATOR BANDWIDTH SIM RESULTS FOR DIFFERENT K=GM_2/GM_1 RATIO

K ratio	Parameter		
	$C_{equivalent}$	f_{-3dB} *simulated*	f_{-3dB} *error*
1	50 pF	478 KHz	0.4%
3	100 pF	266 KHz	0.3%
7	200 pF	143 KHz	0.2%
15	400 pF	75 KHz	0.1%

5. Conclusions

A novel capacitance multiplier scheme that comprises one transconductor cell was presented in this work that comprises a programmable gain factor of 2, 4, 8 and 16. To validate the concept we implemented the proposed schematic in a standard 180nm technology and presented the simulation results. First, we analyzed the equivalent impedance provided by the circuit and found that it emulates a multiplied capacitor over a wide frequency range: the phase error remains below 10 degrees for three decades, from a few kHz to a few MHz. Next, the resulting capacitor was used to implement a triangle-wave generator with adjustable frequency. Finally, a fully differential version of the multiplier was employed to implement a programmable lossy integrator. For both applications the simulation results were very close to expected values, further validating this novel circuit.

Acknowledgments.

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